

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:

Patent No.:

Filed:

Issue Date:

Title:

Commissioner for Patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
(REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patents listed in the table of attachment A,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the listed patents are hereby revoked, and

NEW POWER OF ATTORNEY

the following attorneys/agents are hereby appointed to prosecute this patent/application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this patent/application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number:

15650

Patent Trademark Office

Please direct all future correspondence and telephone calls to:

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ASSIGNEE OF ENTIRE INTEREST

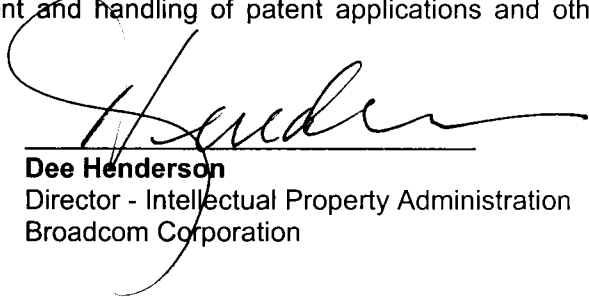
BROADCOM CORPORATION

5300 California Avenue
Irvine, California 92617-3038

ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Broadcom Corporation, I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: 9/12/11



Dee Henderson
Director - Intellectual Property Administration
Broadcom Corporation

Attachment A

No.	Patent No	BD No.	Patent Title	Issue Date	BD Assign't (Reel/Frame)
1	7607052	BU1248.1C1 050228-4880	PHYSICAL CODING SUBLAYER FOR A MULTI-PAIR GIGABIT TRANSCEIVER	10/20/09	010764/0358
2	6259745	BU1256 050228-4890	INTEGRATED GIGABIT ETHERNET TRANSMITTER ARCHITECTURE	07/10/01	010536/0625
3	6898185	BU1261 050228-4900	DIAGNOSTICS OF CABLE AND LINK PERFORMANCE FOR A HIGH-SPEED COMMUNICATION SYSTEM	05/24/05	011594/0614
4	7337375	BU1261C1 050228-4910	DIAGNOSTICS OF CABLE AND LINK PERFORMANCE FOR A HIGH-SPEED COMMUNICATION SYSTEM	02/26/08	011594/0614
5	7711999	BU1261C2 050228-4920	DIAGNOSTICS OF CABLE AND LINK PERFORMANCE FOR A HIGH-SPEED COMMUNICATION SYSTEM	05/04/10	011594/0614
6	7913127	BU1261C3 050228-4930	DIAGNOSTICS OF CABLE AND LINK PERFORMANCE FOR A HIGH-SPEED COMMUNICATION SYSTEM	03/22/11	011594/0614
7	6252904	BU1292 050228-4940	HIGH-SPEED DECODER FOR A MULTI-PAIR GIGABIT TRANSCEIVER	06/26/01	010163/0370
8	6987737	BU1426 050228-4950	PERFORMANCE INDICATOR FOR A HIGH- SPEED COMMUNICATION SYSTEM	01/17/06	011948/0396
9	RE37826	BU1002RE1 050228-4960	ETHERNET SYSTEM	09/03/02	007369/0419
10	6721916	BU1293C1 050228-4970	SYSTEM AND METHOD FOR TRELLIS DECODING IN A MULTI-PAIR TRANSCEIVER SYSTEM	04/13/04	010163/0411
11	7434134	BU1293C2 050228-4980	SYSTEM AND METHOD FOR TRELLIS DECODING IN A MULTI-PAIR TRANSCEIVER SYSTEM	10/07/08	010163/0411
12	6226332	BU1294 050228-4990	MULTI-PAIR TRANSCEIVER DECODER SYSTEM WITH LOW COMPUTATION SLICER	05/01/01	010163/0478
13	6373900	BU1294C1 050228-5010	MULTI-PAIR TRANSCEIVER DECODER SYSTEM WITH LOW COMPUTATION SLICER	04/16/02	010163/0478
14	6944237	BU1294C2 050228-5020	MULTI-PAIR TRANSCEIVER DECODER SYSTEM WITH LOW COMPUTATION SLICER	09/13/05	010163/0478
15	6947482	BU1295C1 050228-5030	SYSTEM AND METHOD FOR HIGH-SPEED DECODING AND ISI COMPENSATION IN A MULTI-PAIR TRANSCEIVER SYSTEM	09/20/05	010163/0561
16	6289047	BU1231 050228-5040	DYNAMIC REGULATION OF POWER CONSUMPTION OF A HIGH-SPEED COMMUNICATION SYSTEM	09/11/01	010228/0504
17	6807228	BU1231C1 050228-5050	DYNAMIC REGULATION OF POWER CONSUMPTION OF A HIGH-SPEED COMMUNICATION SYSTEM	10/19/04	010228/0504

No.	Patent No	BD No.	Patent Title	Issue Date	BD Assign't (Reel/Frame)
18	6477199	BU1231D1 050228-5060	DYNAMIC REGULATION OF POWER CONSUMPTION OF A HIGH-SPEED COMMUNICATION SYSTEM	11/05/02	010228/0504
19	6738419	BU1231D2 050228-5070	DYNAMIC REGULATION OF POWER CONSUMPTION OF A HIGH-SPEED COMMUNICATION SYSTEM	05/18/04	010228/0504
20	6307905	BU1250 050228-5090	SWITCHING NOISE REDUCTION IN A MULTI-CLOCK DOMAIN TRANSCEIVER	10/23/01	010390/0567
21	6959038	BU1292C1 050228-5100	HIGH-SPEED DECODER FOR A MULTI-PAIR GIGABIT TRANSCEIVER	10/25/05	010163/0370
22	6253345	BU1293 050228-5110	SYSTEM AND METHOD FOR TRELLIS DECODING IN A MULTI-PAIR TRANSCEIVER SYSTEM	06/26/01	010163/0411
23	6212225	BU1017 050228-5120	STARTUP PROTOCOL FOR HIGH THROUGHPUT COMMUNICATIONS SYSTEMS	04/03/01	009211/0933
24	6792038	BU1017C1 050228-5130	STARTUP PROTOCOL FOR HIGH THROUGHPUT COMMUNICATIONS SYSTEMS	09/14/04	009211/0933
25	7492813	BU1017C2 050228-5140	STARTUP PROTOCOL FOR HIGH THROUGHPUT COMMUNICATIONS SYSTEMS	02/17/09	009211/0933
26	7020099	BU1018C2 050228-5150	APPARATUS FOR, AND METHOD OF, REDUCING NOISE IN A COMMUNICATIONS SYSTEM	03/28/06	009050/0233
27	6272173	BU1234 050228-5160	EFFICIENT FIR FILTER FOR HIGH-SPEED COMMUNICATION	08/07/01	010393/0128
28	7248629	BU1234C1 050228-5170	EFFICIENT FIR FILTER FOR HIGH-SPEED COMMUNICATION	07/24/07	010393/0128
29	7466751	BU1295C2 050228-5180	SYSTEM AND METHOD FOR HIGH-SPEED DECODING AND ISI COMPENSATION IN A MULTI-PAIR TRANSCEIVER SYSTEM	12/16/08	010163/0561
30	7711077	BU1295C3 050228-5190	SYSTEM AND METHOD FOR HIGH-SPEED DECODING AND ISI COMPENSATION IN A MULTI-PAIR TRANSCEIVER SYSTEM	05/04/10	010163/0561
31	6088354	BU1012 050228-5080	SYSTEM FOR, AND METHOD OF, PROVIDING A HEADER AND A TRAILER IN DATA PACKETS	07/11/00	009092/0113
32	7826446	BU1012C3 050228-5200	SYSTEM FOR AND METHOD OF PROVIDING A HEADER AND A TRAILER IN DATA PACKETS	11/02/10	009092/0113
33	6236645	BU1018 050228-5210	APPARATUS FOR, AND METHOD OF, REDUCING NOISE IN A COMMUNICATIONS SYSTEM	05/22/01	009050/0233
34	6463041	BU1018C1 050228-5220	APPARATUS FOR, AND METHOD OF, REDUCING NOISE IN A COMMUNICATIONS SYSTEM	10/08/02	009050/0233
35	7656827	BU1018C3	APPARATUS FOR, AND METHOD OF, REDUCING NOISE IN A COMMUNICATIONS	02/02/10	009050/0233

No.	Patent No	BD No.	Patent Title	Issue Date	BD Assign't (Reel/Frame)
		050228-5230	SYSTEM		
36	7634001	BU1231C3 050228-5240	DYNAMIC REGULATION OF POWER CONSUMPTION OF A HIGH-SPEED COMMUNICATION SYSTEM	12/15/09	010228/0504
37	7230651	BU2267 050228-5250	A/V DECODER HAVING A CLOCKING SCHEME THAT IS INDEPENDENT OF INPUT DATA STREAMS	06/12/07	013651/0342
38	7702709	BU2284 050228-5260	SYSTEM AND METHOD FOR OPTIMIZING APPROXIMATION FUNCTIONS	04/20/10	013222/0907
39	7263134	BU1247C3 050228-5270	ETHERNET TRANSCEIVER WITH SINGLE-STATE DECISION FEEDBACK EQUALIZER	08/28/07	010694/0029
40	7769101	BU1247C4 050228-5280	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER	08/03/10	010694/0029
41	7224726	BU1573 050228-5290	SYSTEM AND METHOD FOR TERRESTRIAL HIGH-DEFINITION TELEVISION RECEPTION	05/29/07	013015/0832
42	7262806	BU2117 050228-5300	SYSTEM AND METHOD FOR ALIGNED COMPRESSION OF INTERLACED VIDEO	08/28/07	013627/0490
43	7366397	BU2201 050228-5310	V-CHIP DATA PROCESSING FOR DECODER WITH PERSONAL VIDEO RECORDING FUNCTIONALITY	04/29/08	013136/0765
44	7388866	BU2271 050228-5320	SYSTEM AND METHOD FOR EXPEDITING UPPER LAYER PROTOCOL (ULP) CONNECTION NEGOTIATIONS	06/17/08	014084/0760
45	7305007	BU2272 050228-5330	RECEIVER-AIDED SET-UP REQUEST ROUTING	12/04/07	013811/0366
46	7055085	BU2273 050228-5340	SYSTEM AND METHOD FOR PROTECTING HEADER INFORMATION USING DEDICATED CRC	05/30/06	014013/0146
47	6778602	BU1247C1 050228-5350	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER	08/17/04	010694/0029
48	7230652	BU2225.3C1 050228-5360	SYSTEM AND METHOD FOR PROVIDING PICTURE-IN-PICTURE TIMEBASE MANAGEMENT	06/12/07	013185/0763
49	7636834	BU2254 050228-5370	METHOD AND APPARATUS FOR RESETTING A GRAY CODE COUNTER	12/22/09	013671/0456
50	7304652	BU2314C1 050228-5380	SYSTEM AND METHOD FOR PROVIDING GRAPHICS USING GRAPHICAL ENGINE	12/04/07	013331/0625
51	7567261	BU2314C2 050228-5390	SYSTEM AND METHOD FOR PROVIDING GRAPHICS USING GRAPHICAL ENGINE	07/28/09	013331/0625
52	7333447	BU2040 050228-5400	PACKET VOICE SYSTEM WITH FAR-END ECHO CANCELLATION	02/19/08	013797/0648
53	7826718	BU2347 050228-5410	METHOD AND APPARATUS TO FACILITATE THE EFFICIENT IMPLEMENTATION OF TRICK MODES IN A PERSONAL VIDEO	11/02/10	013314/0917

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			RECORDING SYSTEM		
54	7305036	BU2390 050228-5420	SYSTEM AND METHOD FOR ENTROPY CODE PREPROCESSING	12/04/07	014152/0557
55	6819331	BU2253 050228-5430	METHOD AND APPARATUS FOR UPDATING A COLOR LOOK-UP TABLE	11/16/04	013600/0379
56	7420937	Bu2040.1 050228-5440	SELECTIVELY ADAPTABLE FAR-END ECHO CANCELLATION IN A PACKET VOICE SYSTEM	09/02/08	013829/0031
57	7760673	BU2040.1C1 050228-5450	SELECTIVELY ADAPTABLE FAR-END ECHO CANCELLATION IN A PACKET VOICE SYSTEM	07/20/10	013829/0031
58	7333476	BU2040.2 050228-5460	SYSTEM AND METHOD FOR OPERATING A PACKET VOICE FAR-END ECHO CANCELLATION SYSTEM	02/19/08	014424/0832
59	7525918	BU2353 050228-5470	USING RTCP STATISTICS FOR MEDIA SYSTEM CONTROL	04/28/09	013615/0762
60	7477682	BU2354 050228-5480	ECHO CANCELLATION FOR A PACKET VOICE SYSTEM	01/13/09	014481/0633
61	7755641	BU2386 052228-5490	METHOD AND SYSTEM FOR DECIMATING AN INDEXED SET OF DATA ELEMENTS	07/13/10	013360/0103
62	7787539	BU2486 050228-5500	DECODING AND PRESENTATION TIME STAMPS FOR MPEG-4 ADVANCED VIDEO CODING	08/31/10	013797/0384
63	6707848	BU1287C1 050228-5510	DEMODULATOR FOR A MULTI-PAIR GIGABIT TRANSCEIVER	03/16/04	010605/0173
64	6972556	BU1404C1 050228-5520	SYSTEM AND METHOD FOR MEASURING THE POWER CONSUMED BY A CIRCUIT ON A PRINTED CIRCUIT BOARD	12/06/05	011942/0526
65	6714026	BU1404I1 050228-5530	SYSTEM AND METHOD FOR MEASURING THE THICKNESS OR TEMPERATURE OF A CIRCUIT IN A PRINTED CIRCUIT BOARD	03/03/04	012640/0764
66	7002360	BU1404I1C1 050228-5540	SYSTEM AND METHOD FOR MEASURING THE THICKNESS OR TEMPERATURE OF A CIRCUIT IN A PRINTED CIRCUIT BOARD	02/21/06	012640/0764
67	6356273	BU1417C1 050228-5550	Method and system for performing MIP map level selection	03/12/02	??
68	7813431	BU2413 050228-5560	SYSTEM, METHOD, AND APPARATUS FOR DECODING FLEXIBLY ORDERED MACROBLOCKS	10/12/10	013918/0009
69	7127648	BU2529 050228-5570	SYSTEM AND METHOD FOR PERFORMING ON-CHIP SELF-TESTING	10/24/06	013569/0424
70	7093172	BU2530 050228-5580	SYSTEM AND METHOD FOR DETERMINING ON-CHIP BIT ERROR RATE (BER) IN A COMMUNICATION SYSTEM	08/15/06	013748/0929
71	7472318	BU2530C1	SYSTEM AND METHOD FOR DETERMINING ON-CHIP BIT ERROR RATE (BER) IN A	12/30/08	013748/0929

No.	Patent No	BD No.	Patent Title	Issue Date	BD Assign't (Reel/Frame)
		050228-5590	COMMUNICATION SYSTEM		
72	7286622	BU2532 050228-5600	SYSTEM AND METHOD FOR PERFORMING ON-CHIP SYNCHRONIZATION OF SYSTEM SIGNALS UTILIZING OFF-CHIP HARMONIC SIGNAL	10/23/07	014018/0128
73	7463706	BU2532C1 050228-5610	SYSTEM AND METHOD FOR PERFORMING ON-CHIP SYNCHRONIZATION OF SYSTEM SIGNALS UTILIZING OFF-CHIP HARMONIC SIGNAL	12/09/08	014018/0128
74	7656893	BU2537 050228-5620	SYSTEM AND METHOD FOR IMPLEMENTING AUTO-CONFIGURABLE DEFAULT POLARITY	02/02/10	013978/0123
75	7650158	BU4732 050228-5630	SYSTEM AND METHOD FOR SYNCHRONIZING WIRELESS COMMUNICATION DEVICES	01/16/10	017262/0789
76	6927783	BU1208 050228-5640	GRAPHICS DISPLAY SYSTEM WITH ANTI- ALIASED TEXT AND GRAPHICS FEATURE	08/09/05	011361/0918